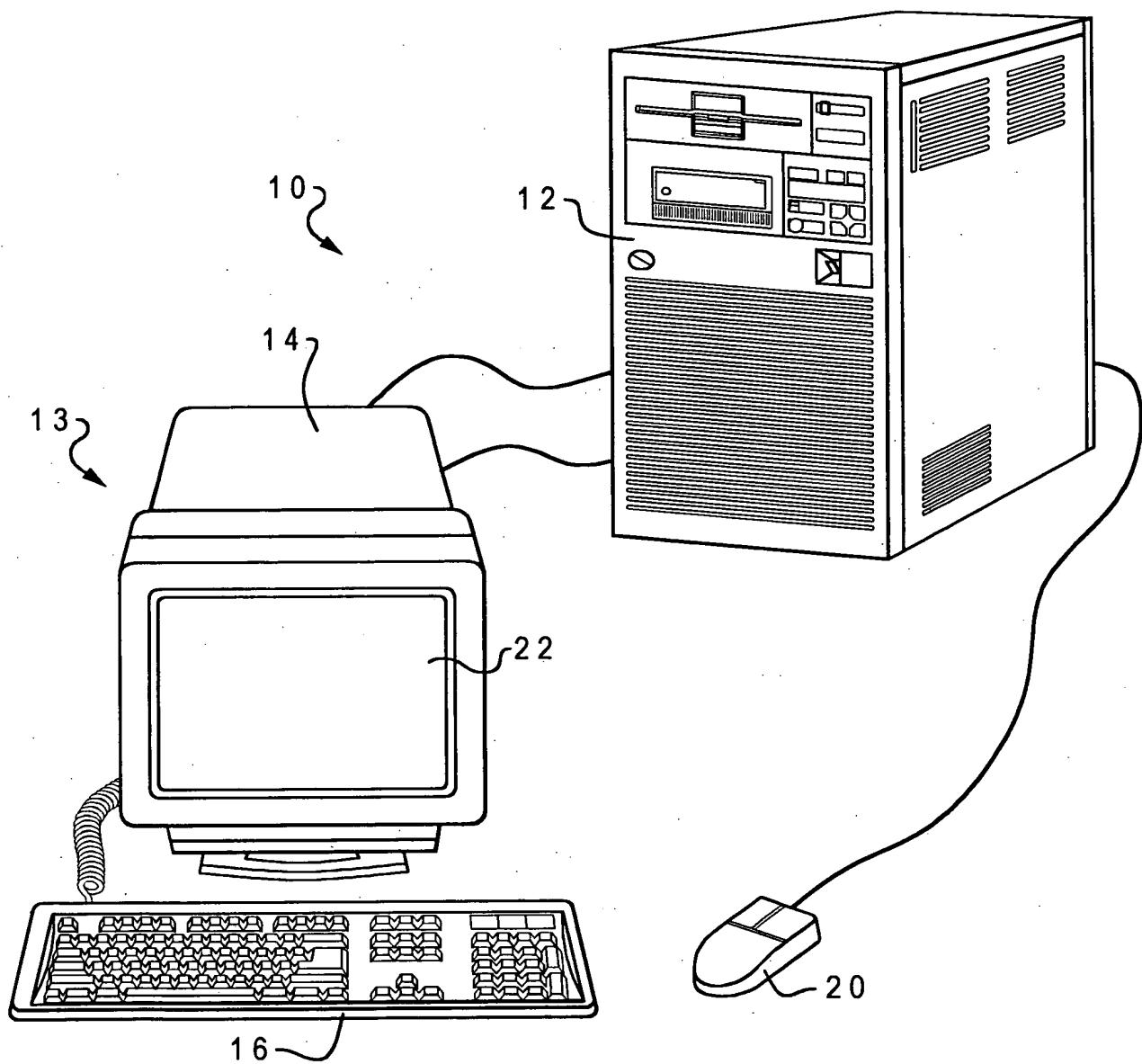
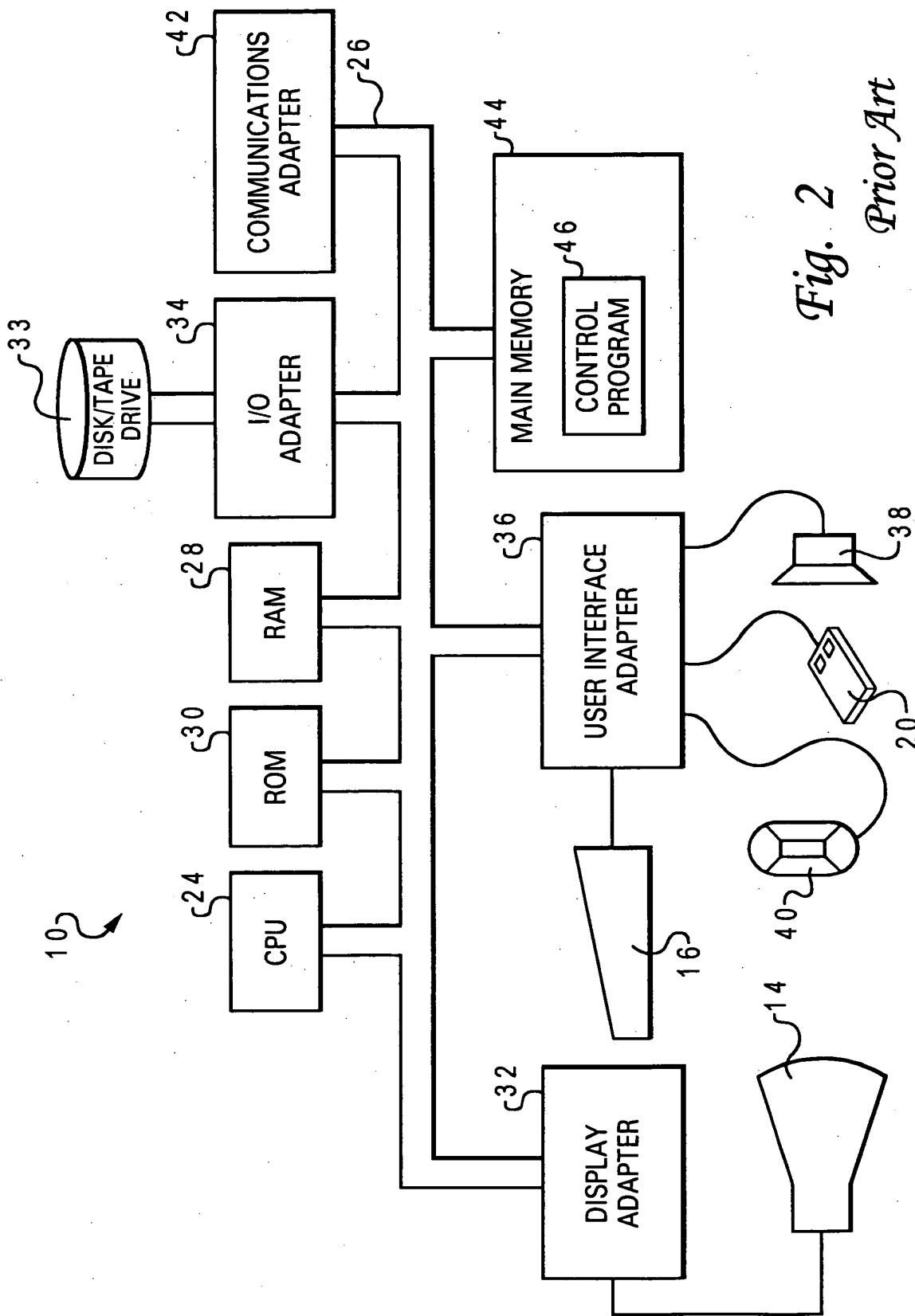


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*Fig. 1
Prior Art*



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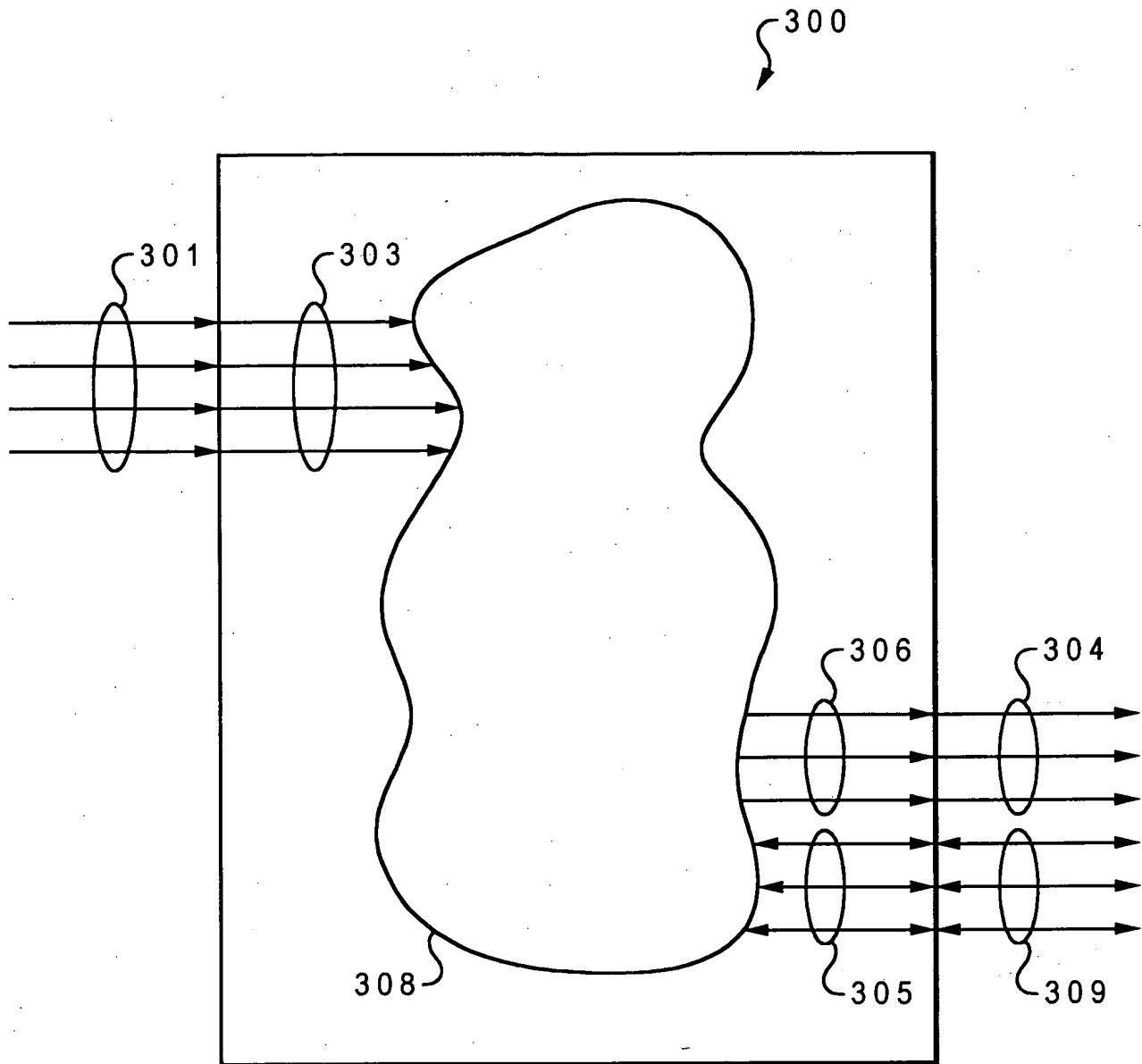


Fig. 3A

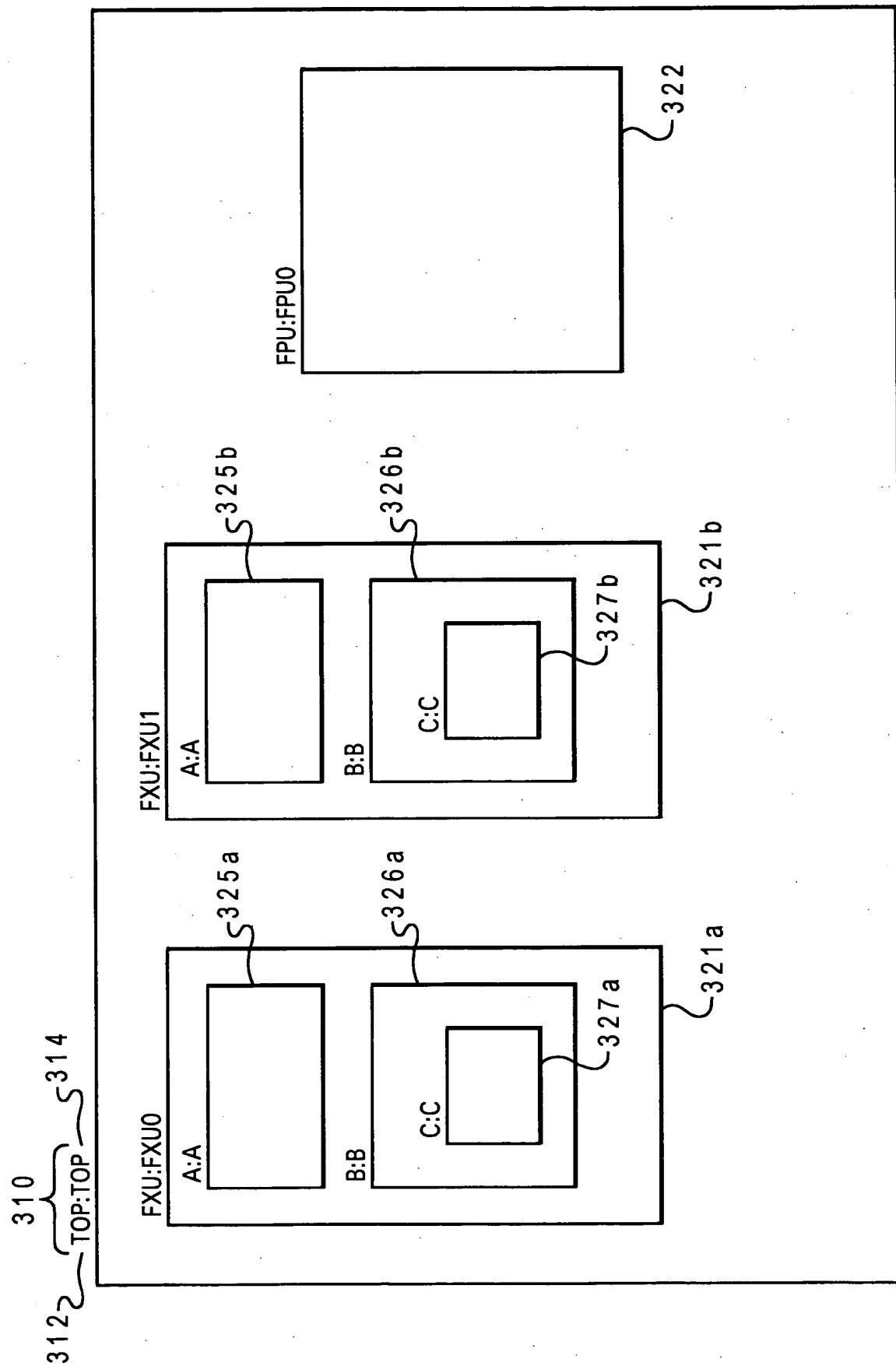


Fig. 3B

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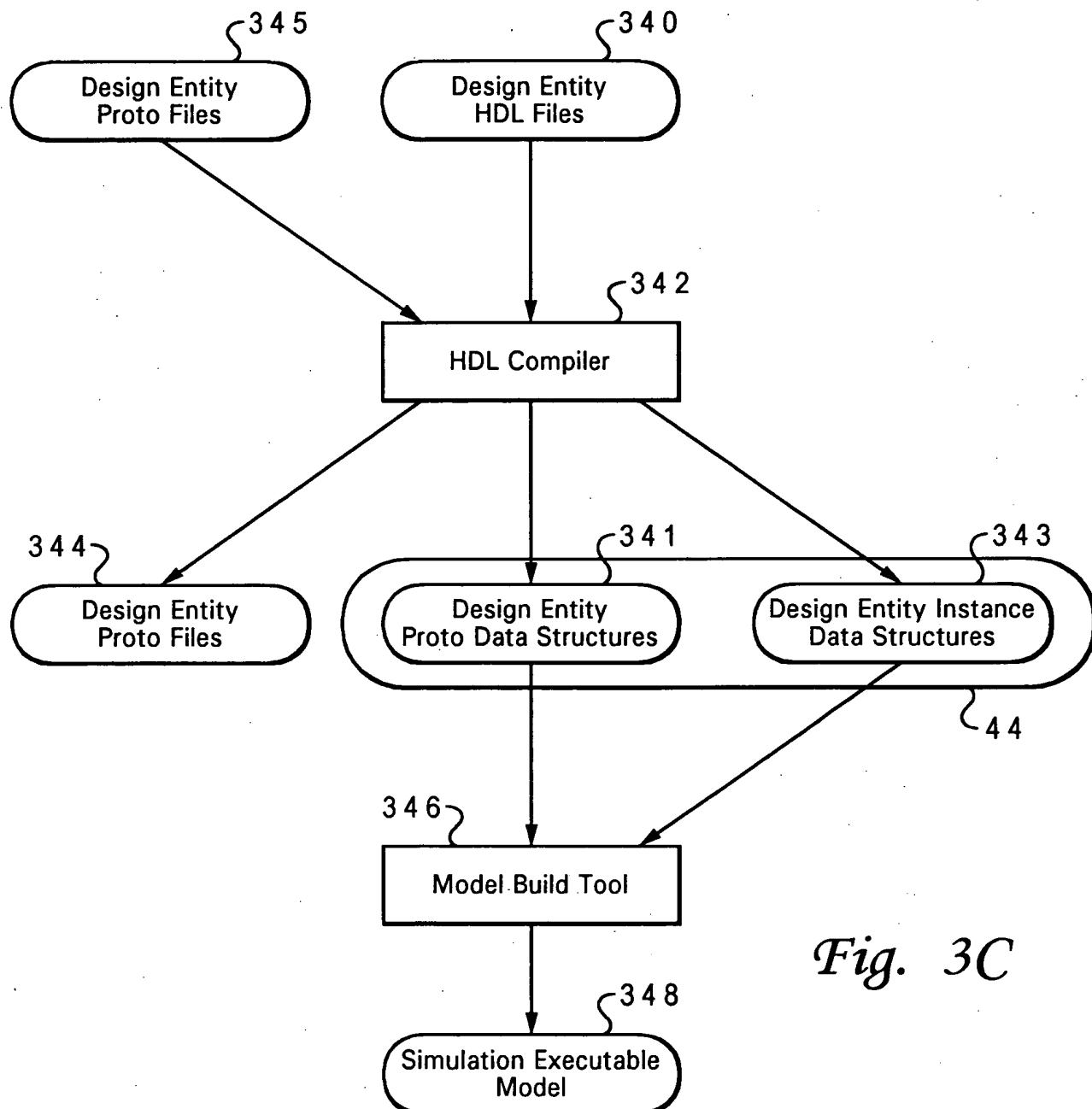


Fig. 3C

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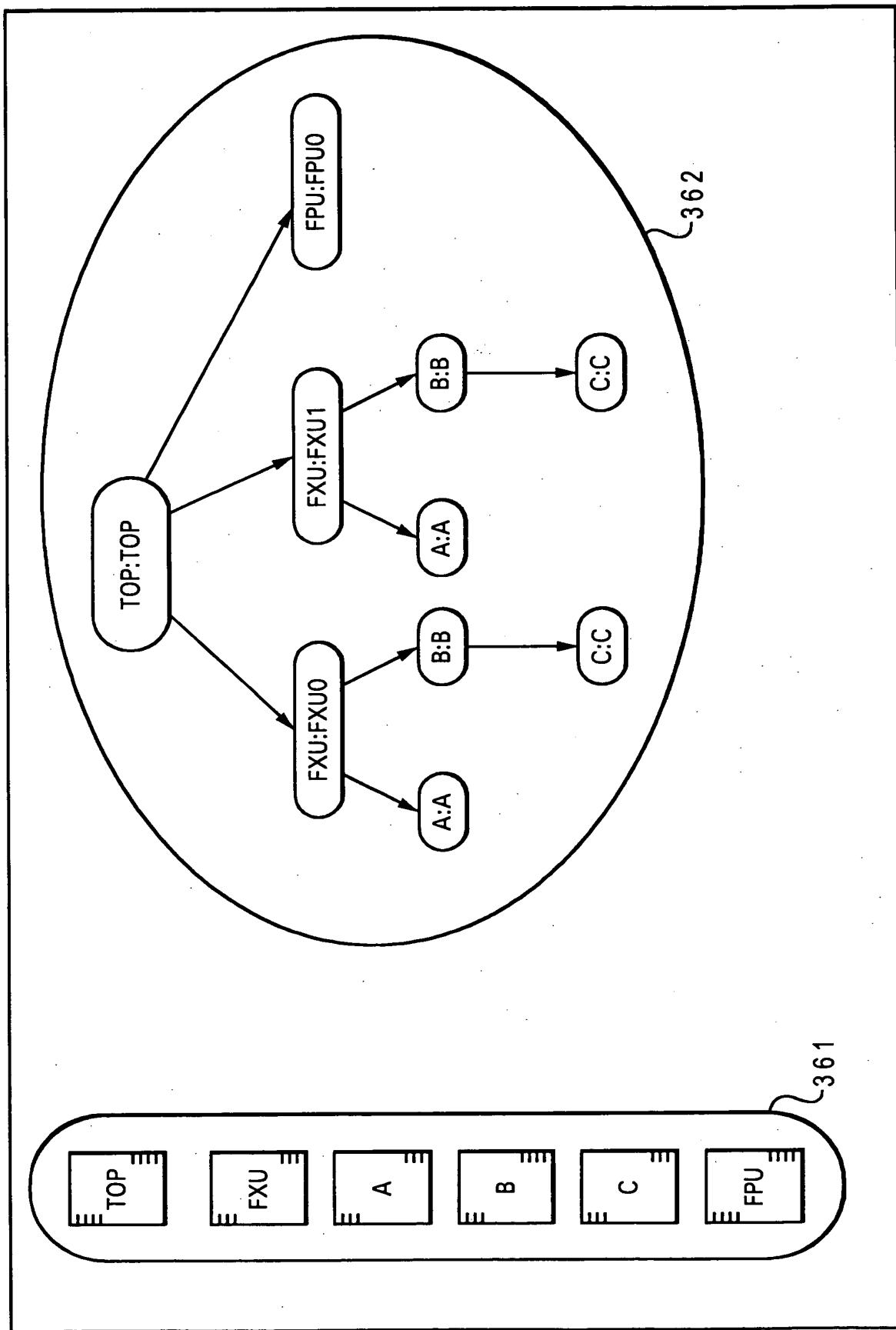


Fig. 3D

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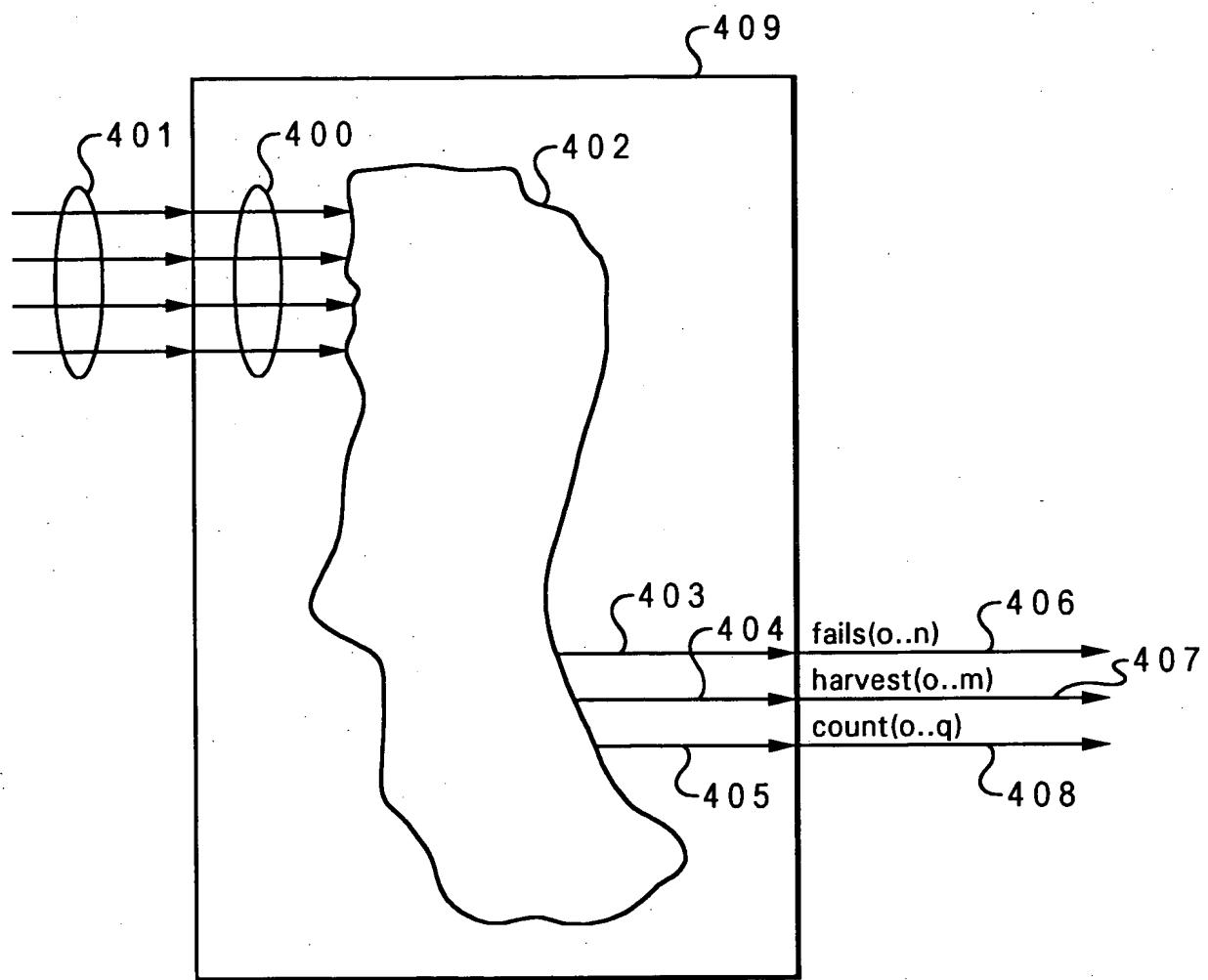


Fig. 4A

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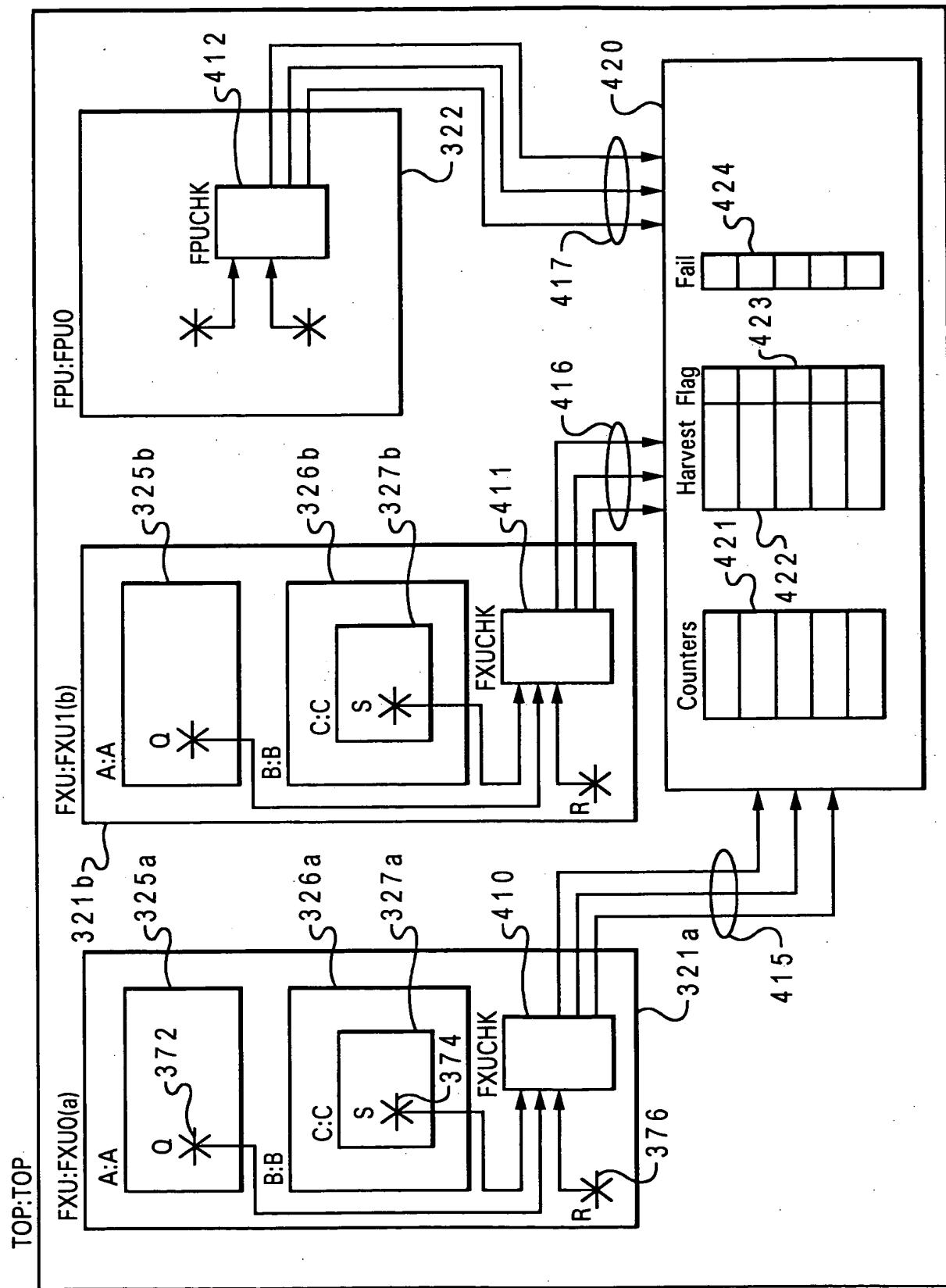


Fig. 4B
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ENTITY FXUCHK IS

```

PORT( S_IN      : IN std_ulogic;
       Q_IN      : IN std_ulogic;
       R_IN      : IN std_ulogic;
       clock     : IN std_ulogic;
       fails     : OUT std_ulogic_vector(0 to 1);
       counts    : OUT std_ulogic_vector(0 to 2);
       harvests  : OUT std_ulogic_vector(0 to 1);
);
    
```

450

452 {
 --!! BEGIN
 --!! Design Entity: FXU;

453 {
 --!! Inputs
 --!! S_IN => B.C.S;
 --!! Q_IN => A.Q;
 --!! R_IN => R;
 --!! CLOCK => clock;
 --!! End Inputs

454 {
 --!! Fail Outputs;
 --!! 0 : "Fail message for failure event 0";
 --!! 1 : "Fail message for failure event 1";
 --!! End Fail Outputs;

455 {
 --!! Count Outputs;
 --!! 0 : <event0> clock;
 --!! 1 : <event1> clock;
 --!! 2 : <event2> clock;
 --!! End Count Outputs;

456 {
 --!! Harvest Outputs;
 --!! 0 : "Message for harvest event 0";
 --!! 1 : "Message for harvest event 1";
 --!! End Harvest Outputs;

457 {
 --!! End;

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ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

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Fig. 4C

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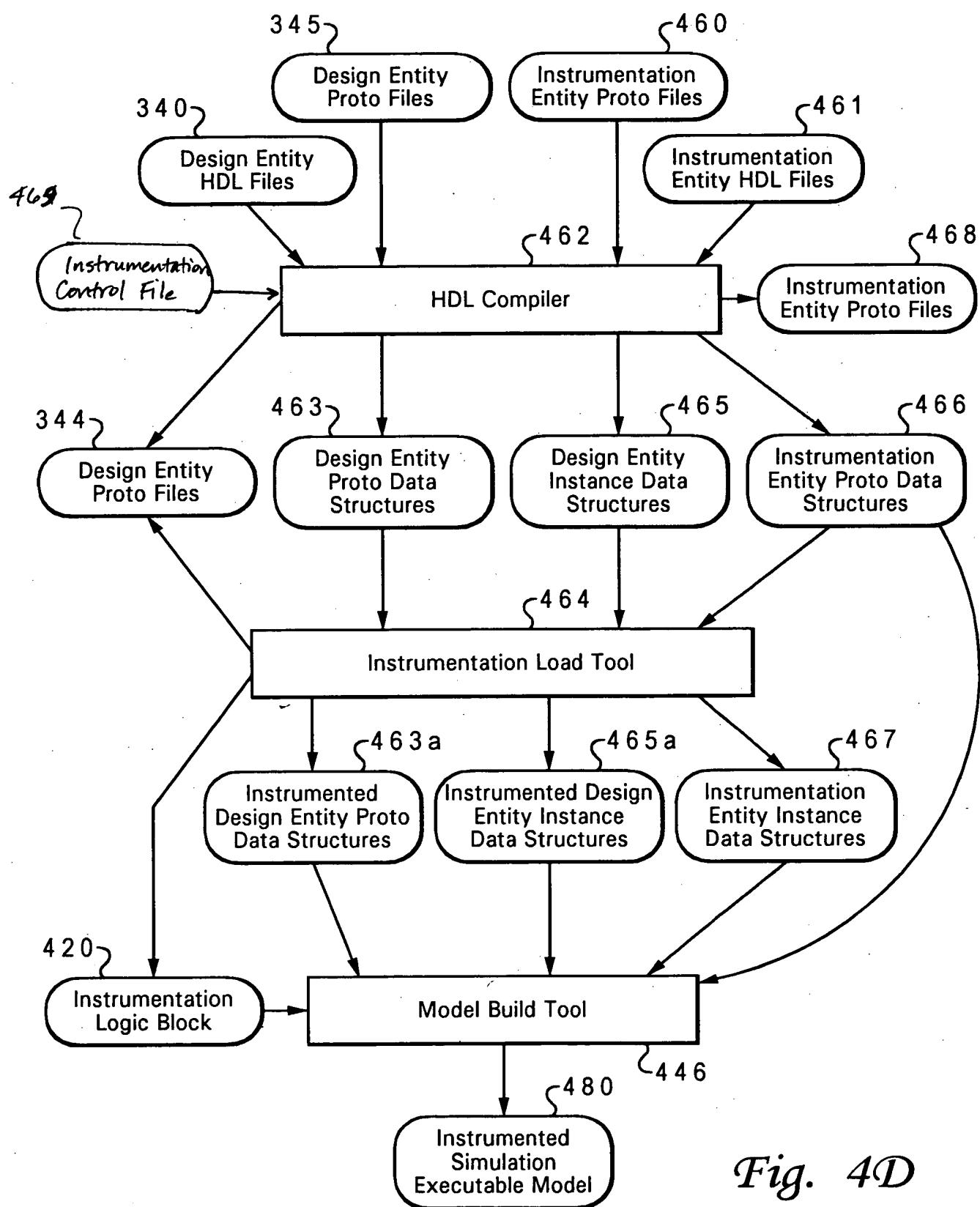


Fig. 4D

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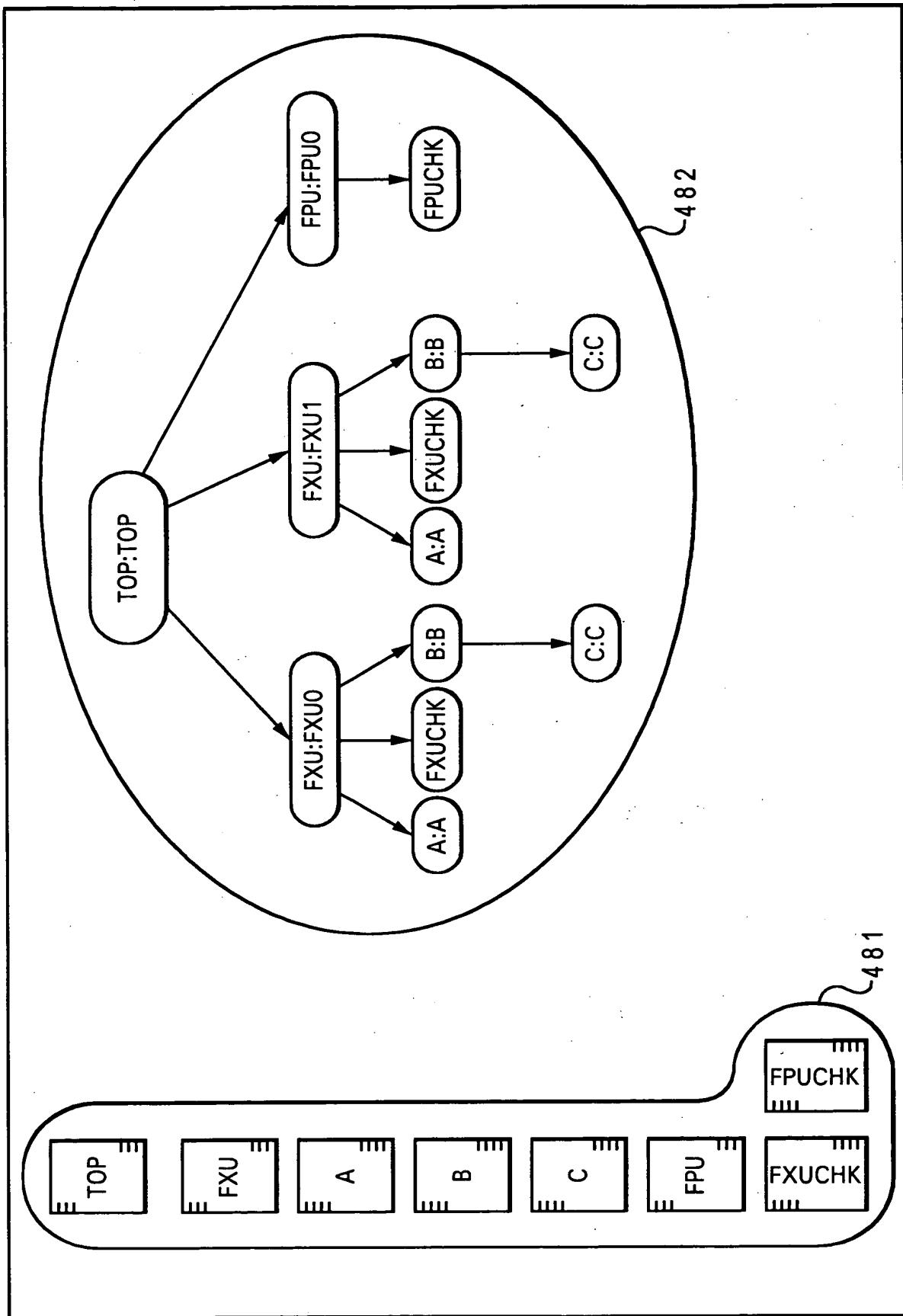


Fig. 4E

FIG. 5

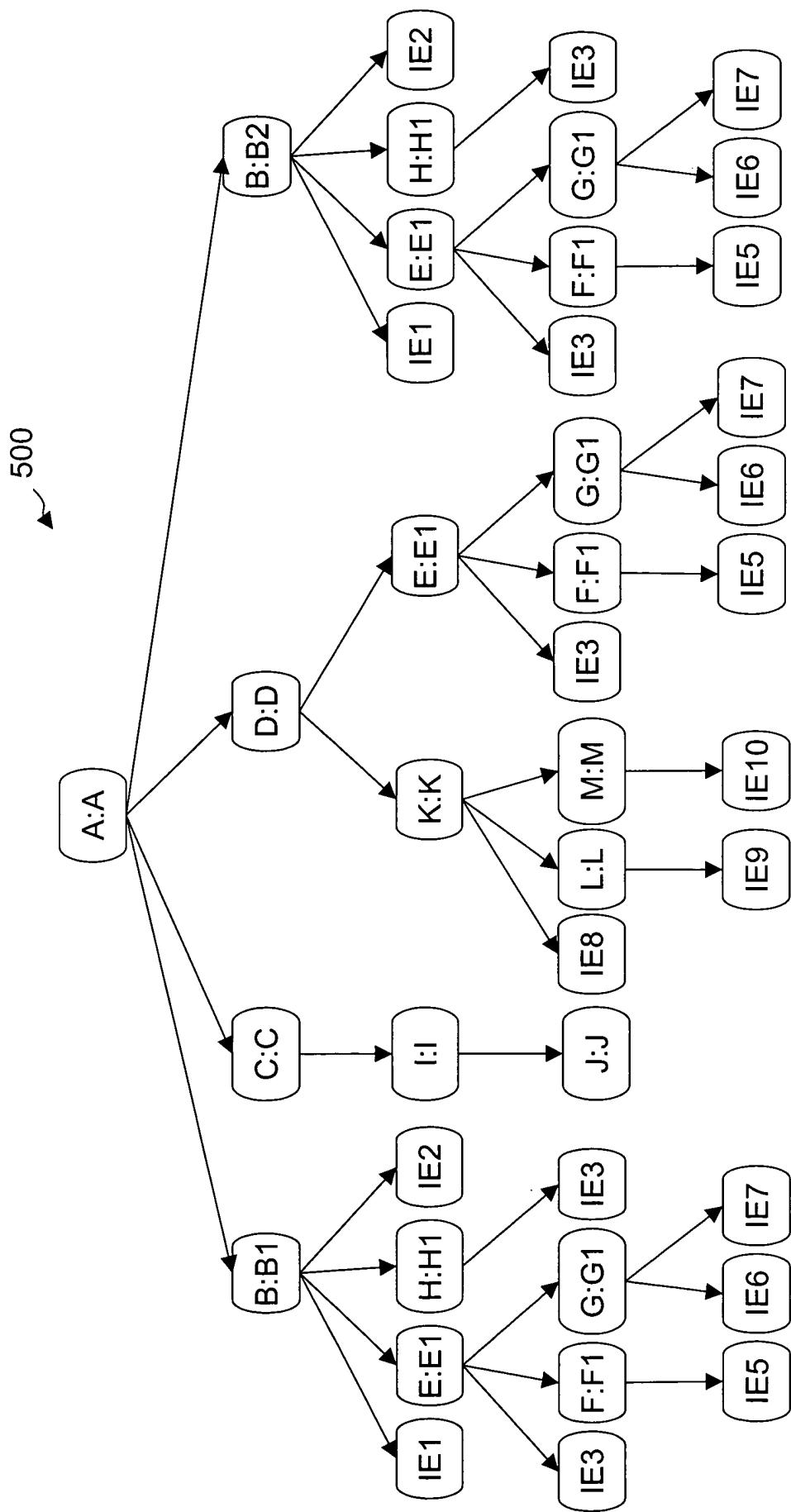


FIG. 6A

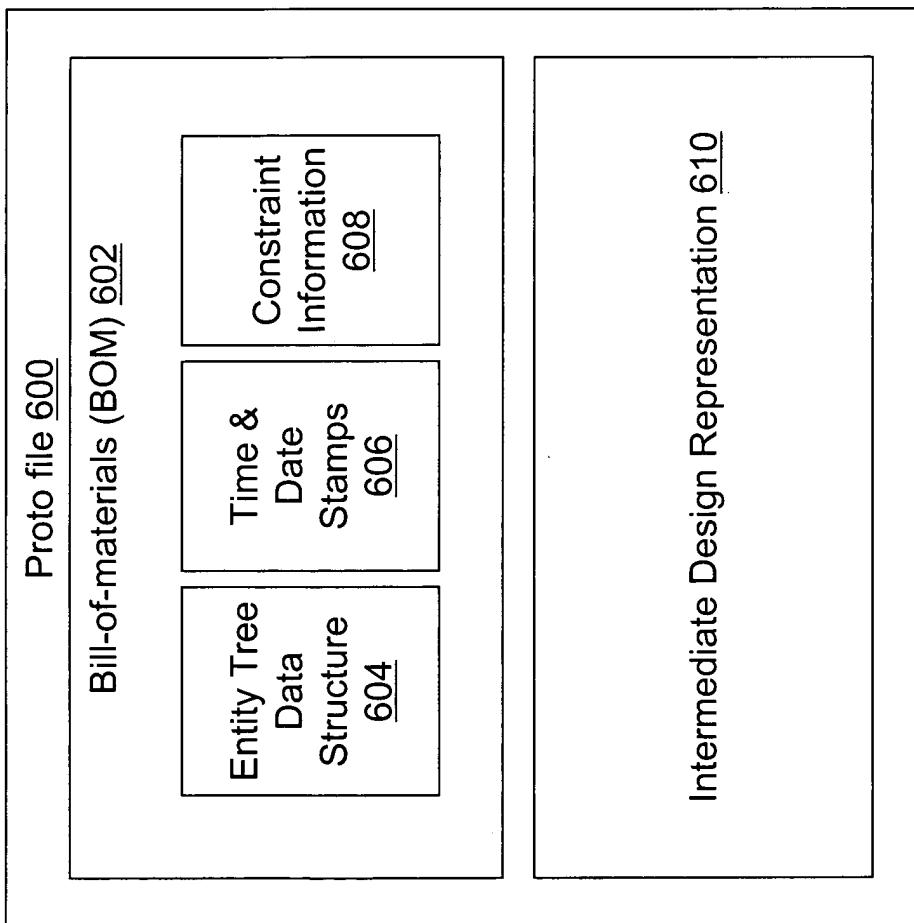


FIG. 6B

| ENTITY | DESCENDANTS |
|--------|--------------------|
| A | B, C, D |
| B | E, H, {IE1}, {IE2} |
| C | I |
| D | K, E |
| E | F, G, {IE3} |
| F | {IE5} |
| G | {IE6}, {IE7} |
| H | {IE4} |
| I | J |
| J | |
| K | L, M, {IE8} |
| L | {IE9} |
| M | {IE10} |

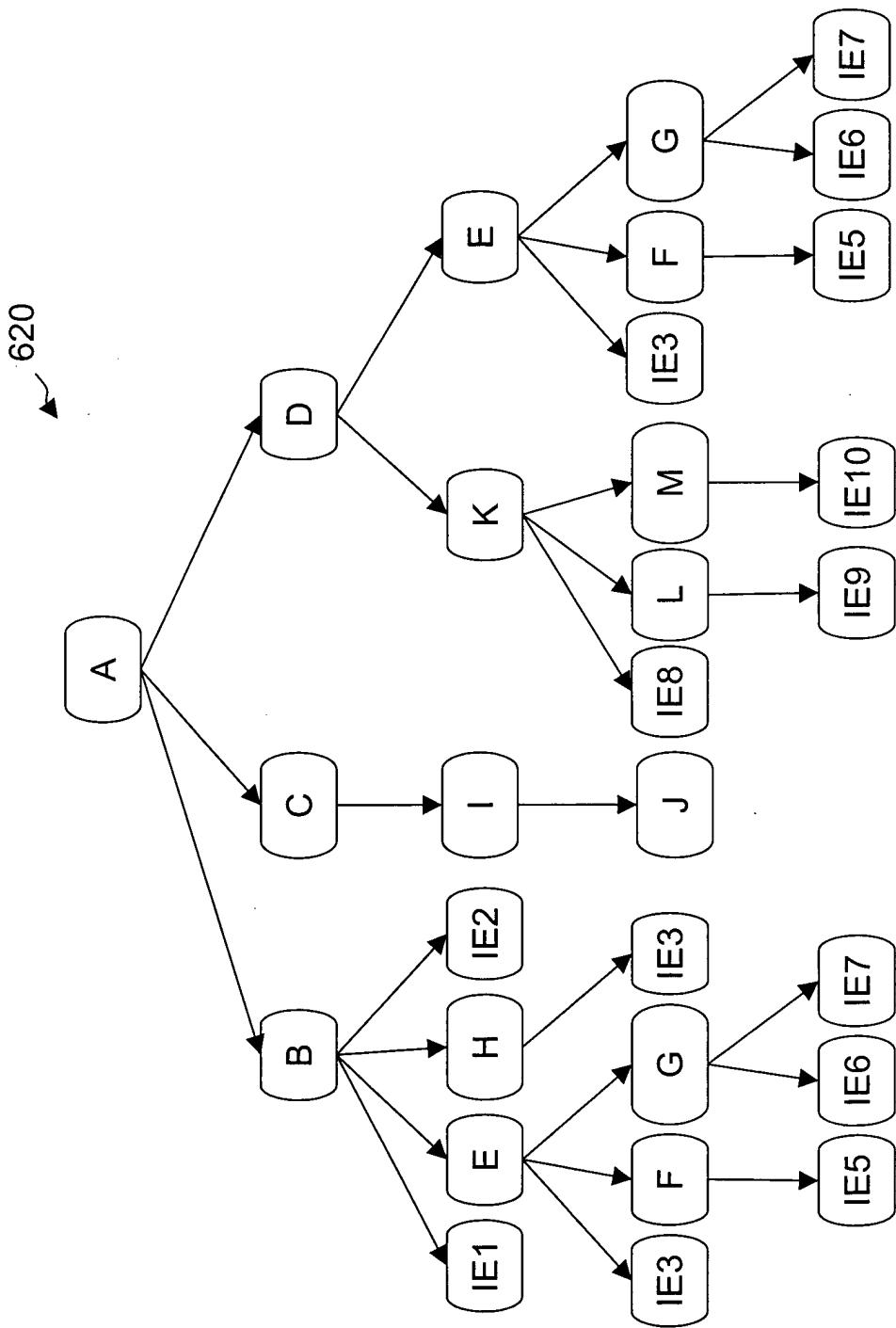
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FIG. 6D

| ENTITY | SELECTED IEs |
|--------|--------------|
| A | |
| B | |
| C | |
| D | |
| E | {IE3} |
| F | {IE5} |
| G | {IE6}, {IE7} |
| H | |
| I | |
| J | |
| K | |
| L | |
| M | |

FIG. 6C



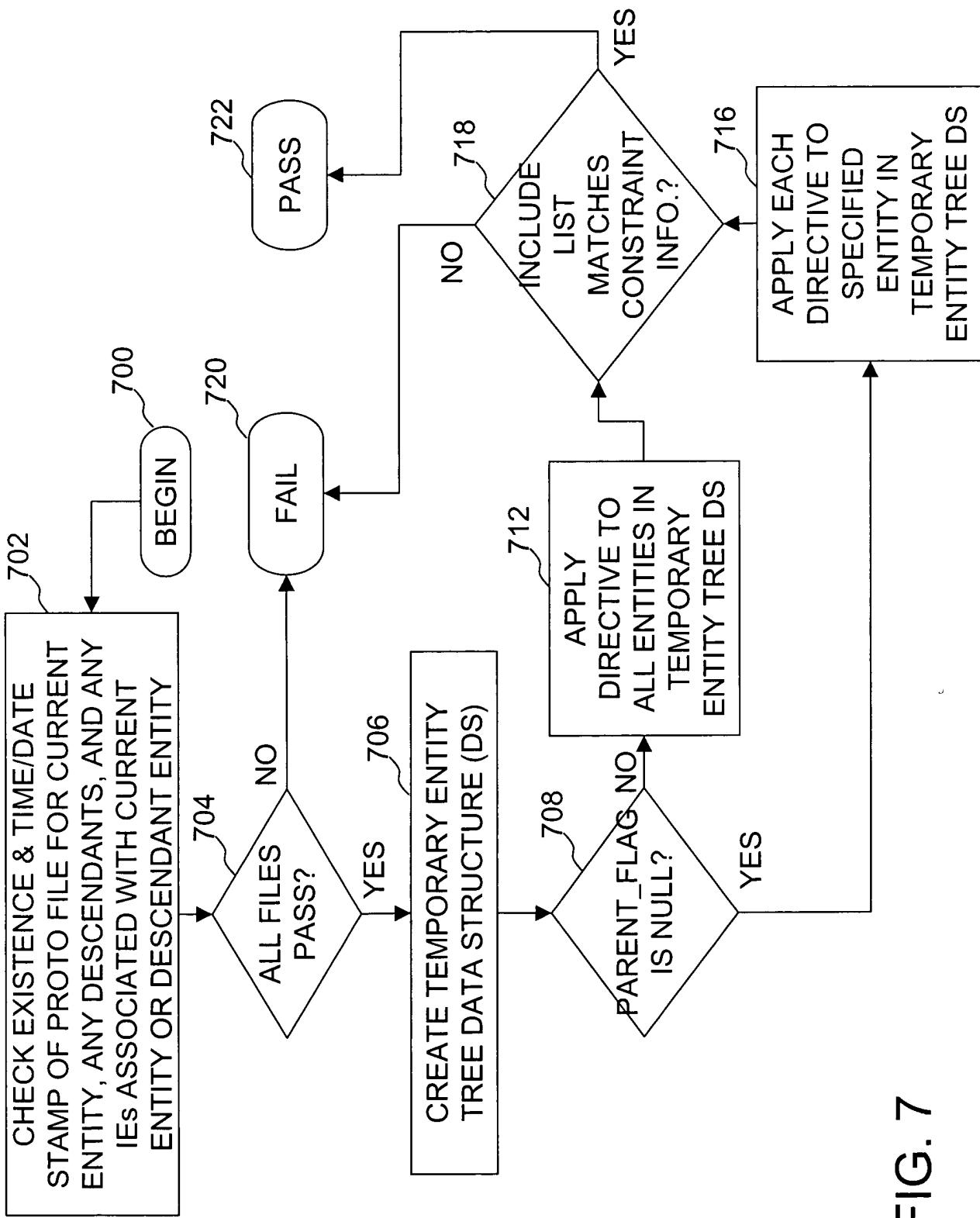


FIG. 7

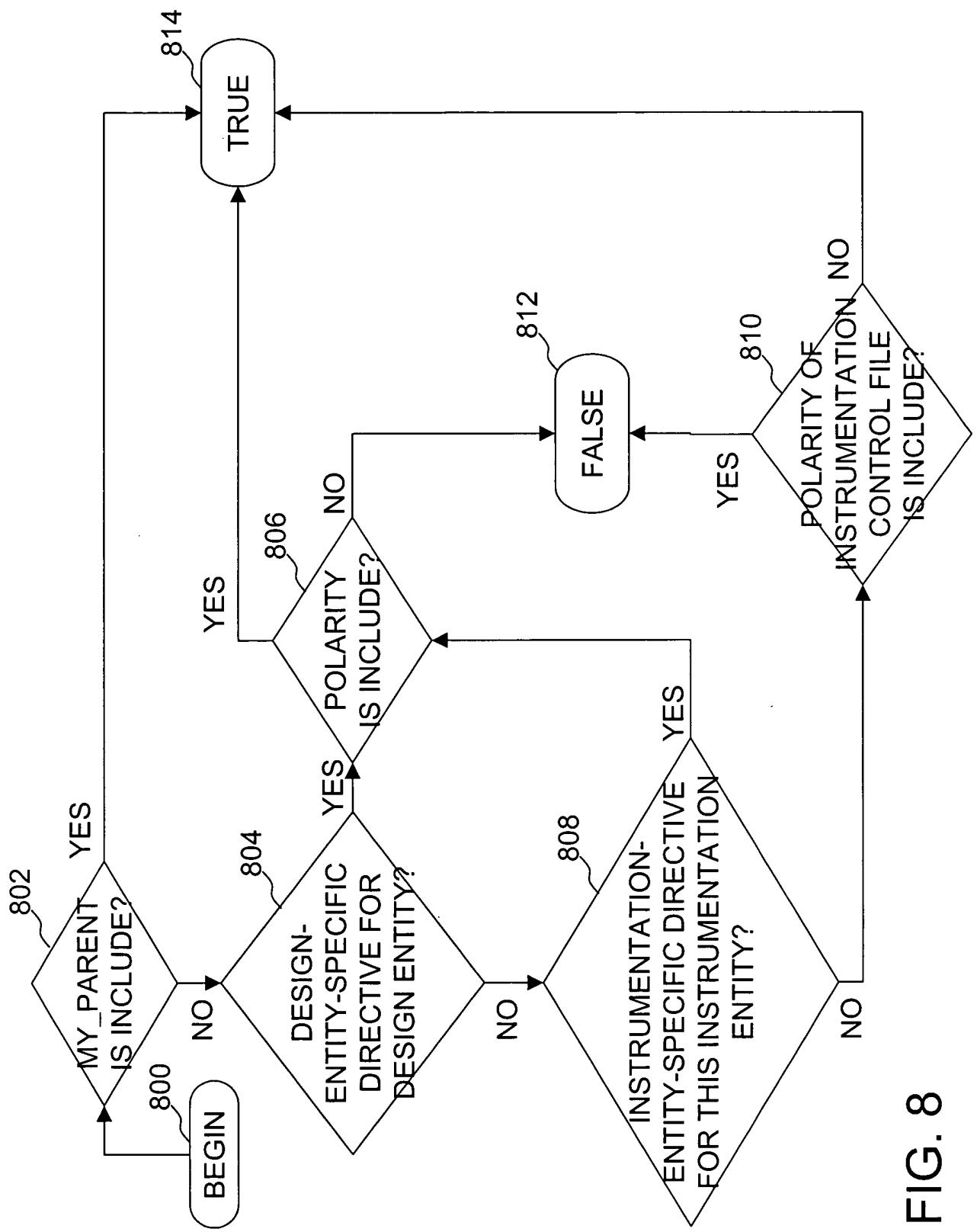


FIG. 8